REMARKS

Claims 1-15 and 27 are pending in the application with new claim 27 added herein.

Page 2 of the Office Action objects to the title as not descriptive. The title is herein amended to clearly indicate the invention to which the claims are directed. Applicants request withdrawal of the objection to the title in the next Office Action.

Claim 2 is objected to under 37 CFR 1.75(c) as being of improper dependent form. Applicants note that claim 2 was amended in a previous response filed March 5, 2002 to set forth that the first electrode "consists of TiN." In contrast, claim 1 sets forth that the first capacitor electrode comprises TiN. Accordingly, claim 2 does not recite the same limitation as claim 1 and is of proper dependent form. Applicants request withdrawal of the claim 2 objection in the next Office Action.

Claims 1-5, 8, and 9 stand rejected under 35 USC 102(e) as being anticipated by Rhodes. Applicants request reconsideration.

Claim 1 sets forth a capacitor fabrication method that includes, among other features, forming a first capacitor electrode containing TiN and having an innermost surface area per unit area and an outermost surface area per unit area that are both greater than an outer surface area per unit area of a substrate under the first capacitor electrode. The method includes forming a capacitor dielectric layer over the first electrode and forming a second capacitor electrode over the dielectric layer. Page 3 of the Office Action alleges that Rhodes teaches a first capacitor electrode having an innermost surface area per unit area greater than an outer surface area per unit area of the substrate. The Office Action refers to column 3, lines 20-23 of Rhodes for support.

However, the recited text does not provide any support whatever for Rhodes teaching a first capacitor electrode having an innermost surface area greater than an outer surface area of the substrate. Rhodes column 3, lines 20-23 merely makes reference to "outermost surface 44." Accordingly, Applicants assert that Rhodes fails to disclose each and every element of claim 1 and does not anticipate claim 1.

Applicants further note that page 3 of the Office Action incorrectly characterizes the first capacitor plate of Rhodes as comprising second layer 42, outermost surface 44 of second layer 42, and layer 46. Rhodes column 3, lines 2-6 clearly state that first layer 40 additionally defines at least a portion of the first capacitor plate. Clearly then, the innermost surface of Rhodes' first capacitor plate constitutes the surface of first layer 40 that contacts insulative layer 34, sidewall spacers 32, and diffusion regions 17 or 21. Such innermost surface of first layer 40 is not described by Rhodes as constituting a roughened surface area such as for outermost surface 44 described in column 3, lines 22-23. The Office Action does not allege and Rhodes does not support any finding that the innermost surface of first layer 40 has a surface area per unit area greater than some portion of the substrate underlying Rhodes' first capacitor plate.

Even taking the incorrect view of the Office that the first capacitor plate includes only second layer 42, outer surface 44 of layer 42, and layer 46 does not yield the structure recited in claim 1. The innermost surface of second layer 42 is the surface that contacts first layer 40. Rhodes does not provide any teaching or even a suggestion that the inner surface of second layer 42 is a roughened surface such as for outermost surface 44 described in column 3, lines 22-23. Thus, Rhodes further does not disclose each and every element of claim 1 and does not anticipate claim 1.

Claims 2-5, 8, and 9 depend from claim 1 and are not anticipated at least for such reason as well as for the additional limitations of such claims not disclosed. For example, claim 2 sets forth that the first electrode consists of TiN. Rhodes column 3, lines 42-44 merely describe layer 46 as possibly including TiN. In contrast, Rhodes does not provide any teaching or even a suggestion that first layer 40 or second layer 42 may include TiN. Since first layer 40 and second layer 42 are part of Rhodes' first capacitor plate, Rhodes does not provide any suggestion of the claim 2 first electrode that consists of TiN.

Also for example, claim 8 sets forth that forming the first electrode includes, among other features, chemisorbing a layer of a first precursor at least one monolayer thick and chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer. A chemisorption product of the first and second precursor layers is comprised by the first electrode. Page 3 of the Office Action alleges that Rhodes teaches "forming a first capacitor electrode comprises TiN monolayer thick [sic]." The Office's statement is unclear, however, the Office does not provide any reference to some portion of Rhodes that can be reasonably considered to disclose the subject matter of claim 8. Rhodes does in any way disclose or suggest forming monolayers. Rhodes does not disclose or suggest chemisorbing a layer of a first precursor and chemisorbing a layer of a second precursor on the first precursor layer. Rhodes does not disclose or suggest any thickness for first layer 40, second layer 42, or layer 46. Rhodes does not disclose or suggest any method for forming first layer 40, second layer 42, or layer 46 that can reasonably be considered suitable for forming a monolayer.

At least for the reasons described herein, claims 1-5, 8, and 9 are not anticipated by Rhodes. Applicants request allowance of such claims in the next Office Action. Applicants

previously asserted in an Office Action response filed March 5, 2002 that 35 U.S.C. 103(c) disqualifies Rhodes from use in forming any obviousness rejection.

Claims 1-15 stand rejected under 35 USC 103(a) as being unpatentable over Chi in view of Wu. Applicants request reconsideration.

The subject matter of claim 1 is described above. Page 5 of the Office Action incorrectly states that the storage node 130a of Wu is "made of TiN" and references column 5, lines 36-38 for support. However, such allegation is in direct contradiction to column 4, lines 55-60 and column 5, lines 13-16 of Wu stating that storage node 130a is made of doped polysilicon. The text of column 5, lines 36-38 referenced by the Office does not in any way suggest substitution of the doped polysilicon of storage node 130a with TiN. Rather, column 5, lines 36-38 only pertains to formation of a seed layer on storage node 130a to provide nucleation sites for later formed HSG silicon layer 131.

Notably, the thin TiN layer is not given a reference numeral in Wu and does not appear in any of Figs. 1-12. It is apparently of minor significance.

It is clear from the thermal oxidation process described in Wu column 5, line 63 to column 6, line 10 and Figs. 11 and 12, that intermittent portions of any TiN seed layer formed on storage node 130a will be removed. Any portion of the TiN layer remaining will be discontinuous, short sections of the original TiN layer between the valleys of the ragged surface formed by the thermal oxidation process and shown in Figs. 11 and 12. Such discontinuous sections of a TiN layer are alone totally unacceptable as a capacitor electrode as clearly known to those of ordinary skill.

Page 5 of the Office Action appears to allege that the thin TiN layer of Wu can be used in place of polysilicon layer 301 of Chi. However, it is a basic requirement of

establishing obviousness by combining references that the Office must show some motivation in the art to support the combination. The only context in which Wu suggests a thin layer is as a seed layer for forming HSG silicon to produce a ragged surface. However, polysilicon layer 301 of Chi already possesses an expanded surface area due to the roughness of sidewalls as described in column 3, lines 23-28. Accordingly, no need exists to add a thin TiN layer as a seed layer on polysilicon layer 301 of Chi. Accordingly, no motivation can be considered to exist to combine a thin TiN layer with the teachings of Chi. Applicants further note that the alternative structure shown in Fig. 5 and described in column 3, lines 45-57 of Chi also possesses an expanded surface area and thus no motivation exists to add a thin TiN layer to such alternative structure.

Since page 5 of the Office Action is very unclear as to exactly what portion of Wu is alleged to modify Chi, Applicants further note that storage node 130a of Wu cannot be substituted for polysilicon layer 301 of Chi. Specifically, claim 1 sets forth that the first capacitor electrode has an innermost surface area per unit area greater than the substrate. In Wu, the portion of storage node 130a shown in Fig. 10 on which HSG silicon layer 131 is formed would constitute the outermost surface of storage node 130a. The innermost surface of storage node 130a constitutes the portion on which HSG silicon layer 131 is not formed (the portion in contact with second dielectric layer 124 and underlying features). Accordingly, it is clear from Wu that such reference does not disclose or suggest an innermost surface area per unit area of storage node 130a that is greater than outermost surface area of the underlying substrate. If storage node 130a of Wu were substituted in the stead of polysilicon layer 301 of Chi, then the resulting combination would fail to disclose or suggest every limitation of claim 1.

At least for the reasons described herein, no motivation exists in the cited art to combine the thin TiN layer of Wu with the teachings of Chi. Additionally, substitution of polysilicon layer 301 of Chi with storage node 130a of Wu would prevent the combination from disclosing or suggesting every element of claim 1. At least for the reasons described herein, claim 1 is patentable over Chi and Wu considered alone or in combination.

Claims 2-9 and 27 depend from claim 1 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. For example, claim 2 sets forth that the first electrode consists of TiN. Neither Chi nor Wu disclose or suggest such a first electrode. Also for example, claim 8 sets forth that forming the first electrode includes chemisorbing a layer of a first precursor at least one monolayer thick and chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer. A chemisorption product of the first and second precursor layers is comprised by the first electrode. Neither Chi nor Wu provide any disclosure or suggestion of chemisorbing first or second precursors, a chemisorption product of the precursors, or any method that may be considered to produce such chemisorption product. Further for example, new claim 27 sets forth that the TiN forms a continuous layer within the first electrode. The subject matter of claim 27 is supported at least by Figs. 4-6 of the present specification and the text associated therewith. Neither Chi nor Wu disclose or suggest TiN as a continuous layer. Only Wu mentions TiN and, as asserted above, such TiN does not form a continuous layer within a first electrode.

Claim 10 sets forth a capacitor fabrication method that includes, among other features, forming an opening in an insulative layer over a substrate, forming a layer of polysilicon over the sides and bottom of the opening, removing the polysilicon layer from

over the bottom of the opening, and converting at least some of the polysilicon layer to hemispherical grain polysilicon. The method includes conformally forming a first capacitor electrode on the HSG polysilicon, the first electrode being sufficiently thin that the first electrode has an outermost surface area per unit area greater than an outer surface area per unit area of the substrate underlying the first electrode. A capacitor dielectric is formed on the first electrode and a second capacitor electrode is formed over the dielectric layer. Page 4 of the Office Action incorrectly alleges that Chi discloses forming a first capacitor electrode on the HSG polysilicon, as set forth in claim 10, and refers to column 1 of Chi for support. However, review of the referenced text does not reveal the alleged subject matter.

Claim 10 expressly states that the first electrode is formed on the HSG polysilicon. By comparison, column 3, lines 4-19 of Chi clearly describe that HSG silicon nodules 203 and amorphous silicon sidewall spacers 201 are completely oxidized. That is, nodules 203 and spacers 201 are entirely converted to silicon dioxide. Accordingly, nodules 203 and spacers 201 do not contain HSG silicon or even amorphous silicon when the heavily doped polysilicon 301 is formed thereon. It is thus impossible for polysilicon 301 to be formed on HSG polysilicon since HSG silicon no longer exists in nodules 203 or even spacers 201.

Nowhere does Chi disclose or suggest that heavily doped polysilicon 301 can be formed on nodules 203 or spacers 201 while such features are still comprised of HSG silicon or amorphous silicon. Wu does not disclose or suggest and the Office Action does not allege that Wu discloses or suggests forming a first capacitor electrode on HSG polysilicon, as set forth in claim 10. Neither Chi nor Wu disclose or suggest such a feature of claim 10. Accordingly, combination of the references cannot be considered to somehow

provide a teaching that is absent from both. At least for such reason, claim 10 is patentable over Chi in view of Wu.

Claims 11-15 depend from claim 10 and are further patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. For example, claim 13 sets forth that forming the first electrode includes chemisorbing a layer of first precursor, chemisorbing a layer of a second precursor, and providing a chemisorption product of the first and second precursor layers that is comprised by the first electrode. Neither Chi nor Wu disclose or suggest the subject matter of claim 13.

Applicants previously asserted in the prior responses to the December 5, 2001 Office Action as well as to the May 10, 2002 Office Action that Chi does not disclose or suggest forming a first capacitor electrode <u>on</u> HSG polysilicon. Even so, the present Office Action persists in not providing any reply to the Applicants' prior assertion and merely repeats the previous incorrect allegation without any justification. Accordingly, the present Office Action is incomplete at least for such reason, warranting withdrawal or correction of the subject claim rejection.

At least for the reasons described herein, claims 1-15 and 27 are patentable over Chi and Wu considered alone or in combination. Applicants request allowance of such claims in the next Office Action.

It is apparent that claims 1-15 discussed herein are not amended and that the Office cannot find that any new ground of rejection will be necessitated by any amendments. The claims as now constituted, with the exception of added claim 27, were previously before the Office and any new ground of rejection must be presented in a non-final rejection.

At least for the reasons described herein, Applicants assert that all of claims 1-15 and 27 are in condition for allowance. Applicants request allowance of such claims in the next Office Action.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO OCTOBER 15, 2002 OFFICE ACTION

In the Specification

The title has been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Enhanced Surface Area Capacitor Fabrication Methods

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